# BTSC PILOT SIGNAL LOCK

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## ABSTRACT OF THE DISCLOSURE

[048] An integrated digital BTSC encoder with an improved pilot signal generator substantially implemented on a single CMOS integrated circuit is described. By digitally generating a sinusoid that is frequency locked to a two-state input reference signal using a high rate internal clock, a hardware-efficient BTSC pilot signal generator is provided with good acquisition and tracking performance. Implemented efficiently as a simple phase detector, a low-complexity loop filter, a pilot frequency offset adder, a phase accumulator and a sinusoidal generator, the invention enables lower-rate post-processing of the pilot tone without a costly variable interpolator decimator structures.